

LSI Logic Corporation Legal Department – IP 1621 Barber Lane, MS D-106 Milpitas, CA 95035

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TC 2825

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From: Connie del Castillo
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REMARKS:				•		
	☐ Urgent	☐ For your review	1	Reply ASAP		Please comment
Application Number: 10/728,036 Filing date: December 3, 2003 First named inventor: Cam Lu et al. Attorney docket number: 03-1978 / 81641  Transmitted herewith for filing via facsimile:  • Status Request Letter						
Pursuant to 37 C.F.R. 1.8, I hereby certify that this correspondence is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date indicated below:    12/15/24   Consider dell Castulo						

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Cam Lu et. al.

Serial No.:

10/728,036

Filed:

December 03, 2003

For:

Method of Generating an Efficeint

Stuck-At Fault and Transition Delay Fault Truncated Scan Test Pattern for an Integrated Circuit Design § § § §

Group Art Unit: 2825

Examiner:

Atty Docket:

81641 / 03-1978

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## STATUS REQUEST

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the status notification to the address stated below.

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Date: 6 DEC OY

Respectfully submitted,

25TR End

Timothy Croll, Ph: [+1] 408-433-7191

Reg. No. 36,771